WHAT IS CLAIMED IS:

1. An etching method comprising:

providing a wafer having a dielectric layer and an electrode partially protruding from a top surface of the dielectric layer;

etching the dielectric layer with a chemical solution; and

prior to etching, reducing the protruding portion of the electrode.

2. The method of claim 1, wherein the protruding portion of the electrode is reduced sufficiently to prevent any bubbles included in the chemical solution from adhering to the electrode.

3. The method of claim 1, wherein reducing the protruding portion comprises recessing a top surface of the electrode below the top surface of the dielectric layer.

4. The method of claim 3, wherein the recessed top surface is at least 500 angstroms below the top surface of the dielectric layer.

5. The method of claim 1, wherein reducing the protruding portion comprises leaving the top surface of the electrode substantially level with the top surface of the dielectric layer.

6. The method of claim1, wherein the top surface of the lower electrode is slightly above the top surface of the dielectric layer such that any bubbles included in the chemical solution can be prevented from adhering to the electrode.

7. The method of claim 1, wherein reducing the protruding portion comprises dry etching.

8. The method of claim 7, wherein drying etching uses an etchant selected from the group consisting of HB_4, Cl_2, CF_4, C_4F_8, C_5F_8, SF_6, O_2 and combinations thereof.

9. The method of claim 1, wherein reducing the protruding portion comprises wet etching.

10. The method of claim 9, wherein wet etching uses a polysilicon etchant.

11. An etching method comprising:

forming a first dielectric layer on a semiconductor substrate;

forming an opening in the dielectric layer;

depositing a conductive layer on the first dielectric layer including the opening;

depositing a second dielectric layer overlying the conductive layer within the opening;

planarizing the resulting structure including the conductive layer, until the top surface of the first layer is exposed, to form a capacitor lower electrode having a top end portion;

reducing the top end portion of the electrode; and

thereafter, etching the first and second dielectric layers with a chemical solution.

12. The method of claim 11, wherein the top end portion of the electrode is reduced such that any bubbles included in the chemical solution do not adhere to the electrode.

13. The method of claim 11, wherein reducing the top end portion comprises recessing a top surface of the electrode below the top surface of the first dielectric layer.

14. The method of claim 13, wherein the recessed top surface is at least 500 angstroms below the top surface of the first dielectric layer.

15. The method of claim 11, wherein reducing the top end portion of the electrode comprises leaving a top surface of the electrode substantially level with the top surface of the first dielectric layer.

16. The method of claim 11, wherein reducing the top end portion of the electrode comprises leaving the top surface of the lower electrode slightly above the top surface of the first dielectric layer such that any bubbles included in the chemical solution can be prevented from adhering to the electrode.

17. The method of claim 11, wherein planarizing comprises chemical mechanical polishing (CMP).

18. The method of claim 17, wherein CMP comprises using a slurry having an etch selectivity between the lower electrode and the dielectric layers.

19. The method of claim 17, wherein reducing the top end portion is performed while performing the CMP.

20. The method of claim 11, wherein planarizing comprises an etching back process.

21. The method of claim 20, wherein reducing the top end portion is performed while performing the etching back process.

22. The method of claim 20, wherein etching back comprises using an etchant having an etch selectivity between the lower electrode and the dielectric layers.

23. The method of claim 11, wherein reducing the top end portion comprises dry etching.

24. The method of claim 23, wherein drying etching uses an etchant selected from the group consisting of HB_4, Cl_2, CF_4, C_4F_8, C_5F_8, SF_6, O_2, and combinations thereof.

25. The method of claim 11, wherein reducing the top end portion comprises wet etching.

26. The method of claim 25, wherein wet etching uses a polysilicon etchant.

27. The method of claim 11, further comprising cleaning the first and second dielectric layers including the electrode to reduce etch residues, after planarizing the resulting structure and before reducing the top end portion of the electrode.

28. The method of claim 27, wherein cleaning comprises using HF.

29. The method of claim 11, wherein the capacitor lower electrode is circular or elliptical in plan view.

30. An etching method comprising:

forming a first dielectric layer on a semiconductor substrate;

forming an opening in the dielectric layer;

depositing a conductive layer on the first dielectric layer including the opening;

depositing a second dielectric layer overlying the conductive layer within the opening;

planarizing the resulting structure including the conductive layer, until the top surface of the first layer is exposed, to form a capacitor lower electrode having a top end portion;

after planarizing the resulting structure, reducing the top end portion of the electrode such that any bubbles included in the chemical solution do not adhere to the electrode; and

thereafter, etching the first and second dielectric layers with a chemical solution.

31. The method of claim 30, wherein reducing the top end portion comprises dry etching.

32. The method of claim 31, wherein drying etching uses an etchant selected from the group consisting of HB_4, Cl_2, CF_4, C_4F_8, C_5F_8, SF_6, O_2, and combinations thereof.

33. The method of claim 30, wherein reducing the top end portion comprises wet etching.

34. The method of claim 33, wherein wet etching uses a polysilicon etchant.

35. The method of claim 30, further comprising cleaning the first and second dielectric layers including the electrode to remove etch residues, after planarizing the resulting structure and before reducing the top end portion of the electrode.

36. The method of claim 35, wherein cleaning comprises using HF.

37. The method of claim 30, wherein the capacitor lower electrode is circular or elliptical in plan view.

38. The method of claim 30, wherein reducing the protruding portion comprises recessing a top surface of the electrode below the top surface of the first dielectric layer.

39. The method of claim 38, wherein the recessed top surface is at least 500 angstroms below the top surface of the first dielectric layer.

40. The method of claim 30, wherein reducing the protruding portion comprises leaving the top surface of the electrode substantially level with the top surface of first the dielectric layer.

41. The method of claim 30, wherein the top surface of the lower electrode is slightly above the top surface of the first dielectric layer such that any bubbles included in the chemical solution can be prevented from adhering to the electrode.